Amendments to the Specification

Please amend the **Specification** as follows:

Please amend paragraph [0001] as follows:

[0001] This application claims priority from provisional application Ser. No. 60/303,247, filed July 6, 2001, which is hereby incorporated by reference in its entirety, and is a continuation of application Ser. No. 10/188,144, filed on July 3, 2002, now U.S. Patent No. 6,678,196, which is hereby incorporated by reference in its entirety.

Please replace paragraphs [0032] and [0033] with the following amended paragraphs [0032] and [0033]:

[0032] The first driver 60_0 ~~70_0~~ is connected to receive bit 0 of write data 0 $WRDI_0$, and its complement $WRDI\_N_0$, a write pulse WRPLS_N, bit line reference BLREF, two control signals PCC, NCC and a read pulse RDPLS_N. It should be noted that $WRDI_0$ and $WRDI\_N_0$ do not have to be complements. In certain circumstances, such as when a write operation is completed, it is desirable to have both $WRDI_0$ and $WRDI\_N_0$ set to a low level. Typically, it is not desirable to have both $WRDI_0$ and $WRDI\_N_0$ set to a high level. Thus, the combination of the $WRDI_0$ and $WRDI\_N_0$ can have three states.

[0033] The first driver 60_0 ~~70_0~~ uses the input write data $WRDI_0$, and its complement $WRDI\_N_0$, to drive a first bit line 26_0 and a second bit line 28_0. The bit lines 26_0, 28_0 are connected to an SRAM cell 10 in each array of words WORD 0, WORD 1 to WORD n. The other drivers 60_m ~~70_m~~ receive other bits of the write data (e.g., $WRDI_m$ and $WRDI\_N_m$) and use the data to drive other first and second